Abstract

As the industry reaps the benefits of Moore's Law and chip designs increase in complexity, System-on-Chip (SoC) integration is becoming intractable with the advent of many new bus or interface protocols. As a case study, this paper proposes a self-organization algorithm for designing high-efficiency SBUS wrappers in order to interconnect third-party Intellectual Properties (IPs) and find a right balance between system performance and resource cost. Field-programmable gate array (FPGA) results show large reduction in our self-integration system's area and energy consumption (77.6% in block tests), compared with the AXI3 SoC. Additionally our proposed work achieves higher valid throughput (up to 1.2×) than the AXI3 implementation.